WHAT IS CLAIMED IS:

1. A method of operation of a module that includes a plurality of integrated circuit dies and a programmable memory device disposed within a housing, wherein the method comprises:

determining a set of integrated circuit dies, of the plurality of integrated circuit dies, that meets a predetermined standard, wherein at least one integrated circuit die of the plurality of integrated circuit dies not included in the set of integrated circuit dies does not meet the predetermined standard; and

programming the programmable memory device to identify the set of integrated circuit dies that meets the predetermined standard.

2. The method according to claim 1, wherein said predetermined standard includes a predetermined operating frequency.

3. The method according to claim 1, wherein said predetermined standard includes a predetermined core timing grade.

4. The method according to claim 1, wherein said predetermined standard includes whether an integrated circuit die is functioning.

5. The method according to claim 1, further comprising, prior to said determining, stacking said plurality of integrated circuit dies adjacent to one another.

6. The method according to claim 1, wherein said programming comprises programming fuses.

7. The method according to claim 1, wherein said programming comprises programming a read only memory (ROM) integrated circuit chip.

8. The method according to claim 1, wherein said programming comprises programming a read/write integrated circuit chip.

9. The method according to claim 1, wherein said programming comprises programming an erasable programmable read-only memory (EPROM).

10. A method of operation of a module that includes a plurality of integrated circuit dies and a programmable memory device disposed within a housing, wherein the method comprises:

establishing a first integrated circuit die, of the plurality of integrated circuit dies, that meets a predetermined standard, wherein a second integrated circuit die of the plurality of integrated circuit dies does not meet the predetermined standard; and

programming the programmable memory device to identify the first integrated circuit die.

11. The method according to claim 10, wherein said predetermined standard includes a predetermined operating frequency.

12. The method according to claim 10, wherein said predetermined standard includes a predetermined core timing grade.

13. The method according to claim 10, wherein said predetermined standard includes whether an integrated circuit die is functioning.

14. The method according to claim 10, further comprising, prior to said determining, stacking said plurality of integrated circuit dies adjacent to one another.

15. A method of operation of a module that includes a plurality of integrated circuit dies and a programmable memory device disposed within a housing, wherein the method comprises:

determining which of the plurality of integrated circuit dies are functioning circuit dies and which are non-functioning circuit dies; and

programming the programmable memory device to identify the functioning circuit dies.

16. The method according to claim 15, further comprising:

determining an operating frequency for each of said functioning circuit dies;

identifying which operating frequency is a lowest operating frequency; and

storing in the programmable memory device, the lowest operating frequency as a maximum operating frequency for the module.

17. The method according to claim 15, further comprising:

determining a core timing grade for each of said functioning circuit dies;

identifying which core timing grade is a lowest core timing grade; and

storing in the programmable memory device, the lowest core timing grade as a maximum core timing grade for the module.

18. The method according to claim 15, further comprising, prior to said determining, stacking said plurality of integrated circuit dies adjacent to one another.

19. The method according to claim 15, wherein said programming comprises programming fuses.

20. The method according to claim 15, wherein said programming comprises programming a read only memory (ROM) integrated circuit chip.

21. The method according to claim 15, wherein said programming comprises programming a read/write integrated circuit chip.

22. The method according to claim 15, wherein said programming comprises programming an erasable programmable read-only memory (EPROM).

23. A method of operation of a module that includes a plurality of integrated circuit dies and a programmable memory device disposed within a housing, wherein the method comprises:

determining which of the plurality of integrated circuit dies meet a predetermined standard and which of the plurality of integrated circuit dies do not meet the predetermined standard; and

programming the programmable memory device to identify the integrated circuit dies that meet the predetermined standard.

24. The method according to claim 23, wherein said predetermined standard includes a predetermined operating frequency.

25. The method according to claim 23, wherein said predetermined standard includes a predetermined core timing grade.

26. The method according to claim 23, wherein said predetermined standard includes whether an integrated circuit die is functioning.

27. The method according to claim 23, further comprising, prior to said determining, stacking said plurality of integrated circuit dies adjacent to one another.

28. The method according to claim 23, wherein said programming comprises programming fuses.

29. The method according to claim 23, wherein said programming comprises programming a read only memory (ROM) integrated circuit chip.

30. The method according to claim 23, wherein said programming comprises programming a read/write integrated circuit chip.

31. The method according to claim 23, wherein said programming comprises programming an erasable programmable read-only memory (EPROM).

32. The method according to claim 23, wherein said determining further comprises:

determining a core timing grade for each of said circuit dies that meet the predetermined standard;

identifying which core timing grade is a lowest core timing grade; and

storing in the programmable memory device, the lowest core timing grade as a maximum core timing grade for the module.

33. The method according to claim 23, wherein said determining further comprises:

determining an operating frequency for each of said circuit dies that meet the predetermined standard;

identifying which operating frequency is a lowest operating frequency; and

storing in the programmable memory device, the lowest operating frequency as a maximum operating frequency for the module.

34. A method of operation of a module that includes a plurality of integrated circuit memory devices and a programmable memory device disposed within a housing, wherein the method comprises:

determining a core timing grade for each of said plurality of integrated circuit memory devices;

identifying which core timing grade is a lowest core timing grade; and

storing in the programmable memory device, the lowest core timing grade as a maximum core timing grade for the module.

35. The method according to claim 34, wherein said determining only occurs for those integrated circuit memory devices of said plurality of integrated circuit memory devices that function.

36. The method according to claim 34, wherein said identifying only occurs for those integrated circuit memory devices of said plurality of integrated circuit memory devices that meet a threshold core timing grade.

37. The method according to claim 34, wherein said storing comprises programming fuses, a read only memory (ROM) integrated circuit chip, a read/write integrated circuit chip, or an erasable programmable read-only memory (EPROM).

38. A method of operation in a module that includes a plurality of integrated circuit memory devices and a programmable memory device disposed within a housing, wherein the method comprises:

determining an operating frequency for each of said plurality of integrated circuit memory devices;

identifying which operating frequency is a lowest operating frequency; and

storing in the programmable memory device, the lowest operating frequency as a maximum operating frequency for the module.

39. The method according to claim 38, wherein said determining only occurs for those integrated circuit memory devices of said plurality of integrated circuit memory devices that function.

40. The method according to claim 38, wherein said identifying only occurs for those integrated circuit memory devices of said plurality of integrated circuit memory devices that meet a threshold operating frequency.

41. The method according to claim 38, wherein said storing comprises programming fuses, a read only memory (ROM) integrated circuit chip, a read/write integrated circuit chip, or an erasable programmable read-only memory (EPROM).

42. A method of operation of a memory module that includes a plurality of integrated circuit dies and a programmable memory device disposed within a housing, wherein the method comprises storing in the programmable memory device a lowest core timing grade, of all core timing grades of the plurality of integrated circuit memory devices, as a maximum core timing grade for the memory module.

43. A method of operation of a memory module that includes a plurality of integrated circuit dies and a programmable memory device disposed within a housing, wherein the method comprises storing in the programmable memory device a lowest operating frequency, of all operating frequencies of the plurality of integrated circuit memory devices, as a maximum operating frequency for the memory module.

44. A semiconductor module, comprising:

a unitary housing;

a plurality of integrated circuit dies positioned within said unitary housing;

a means for determining which integrated circuit dies of the plurality of circuit dies meet a predetermined standard, and which integrated circuit dies of the plurality of circuit dies do not meet the predetermined standard; and

a programmable means for identifying the integrated circuit dies that meet the predetermined standard, where said programmable means is also positioned within said unitary housing.

45. The semiconductor module according to claim 44, wherein said means for determining further ascertains a maximum operating frequency and maximum core timing grade for said semiconductor module.

46. The semiconductor module according to claim 44, wherein said predetermined standard is whether an integrated circuit die functions.

47. The semiconductor module according to claim 44, wherein said programming means includes: a system of fuses, a read only memory (ROM) integrated circuit chip, a read/write integrated circuit chip, or an erasable programmable read-only memory (EPROM).